IN THE CLAIMS

Please amend the claims as follows:

1. (original) A receiver (1, 49, 51, 52, 54) with a signal path comprising the following elements: a tuning arrangement (49), a demodulator circuit (51) for supplying a stereo multiplex signal with a baseband stereo sum signal (L+R), a 19 kHz stereo pilot and a stereo difference signal (L-R) double-sideband amplitude-modulated on a blanked 38 kHz subcarrier, a sampling arrangement (52) for converting an analog signal into a time-discrete signal, and a stereo decoder (1) with a filter (2, 4, 7, 8, 9) and a phase-locked loop (80) comprising an oscillator (19), characterized in that filter operations can be performed in a complex range.

2. (original) A receiver as claimed in claim 1, characterized in that the filter (2, 4, 7, 8, 9) is complex.

3. (currently amended) A receiver as claimed in claim 1 ~~or 2~~, characterized in that the complex filter (2, 4, 7, 8, 9) is a finite impulse response filter (2, 4, 7, 8, 9).

4. (original) A receiver as claimed in claim 1, characterized in that the oscillator (19) is discrete-controlled.

5. (currently amended) A receiver as claimed in claim 1~~ or 4~~, characterized in that the oscillator (19) supplies a complex signal.

6. (currently amended) A receiver as claimed in claim 1~~, 4 or 5~~, characterized in that the oscillator (19) supplies a cosine signal and a sine signal.

7. (currently amended) A receiver as claimed in ~~any one of the preceding claims~~claim 1, characterized in that the oscillator (19) comprises a limit-stable oscillating filter.

8. (currently amended) A receiver as claimed in ~~any one of the preceding claims~~claim 1, characterized in that the oscillator (19) controls a modulator (3, 5, 10, 11).

9. (original) A receiver as claimed in claim 8, characterized in that the modulator (3, 5, 10, 11) comprises a multiplying member.

10. (original) A receiver as claimed in claim 1, characterized in that the sampling arrangement (52) operates at a fixed clock.

11. (original) A receiver as claimed in claim 10, characterized in that the fixed clock is between 4 x 20 kHz and 4 x 80 kHz, advantageously between 4 x 32 kHz and 4 x 64 kHz, particularly at 4 x 44.1 kHz.

12. (original) A receiver as claimed in claim 1, characterized in that the stereo pilot is filtered with an elliptic filter (16) having a frequency response around 0 Hz.

13. (original) A receiver as claimed in claim 1, characterized in that the stereo decoder (1) comprises a converter (14, 15) which converts complex signals to real signals.

14. (original) A receiver as claimed in claim 1, characterized in that the phase-locked loop (80) comprises a control path (17) with an amplifier (81, 83).

15. (original) A method of decoding a time-discrete stereo multiplex signal with a baseband stereo sum signal (L+R), a 19 kHz stereo pilot and a stereo difference signal (L-R) double-sideband amplitude-modulated on a blanked 38 kHz subcarrier in a decoder of a receiver, characterized by the steps of

- filtering the stereo multiplex signal by means of a filter, in which one of the two stereo signals (L+R, L-R) is complex-filtered by means of a slope,
- complex-modulating the filtered signal by means of a modulator,
- filtering the modulated signal by means of a filter, in which the other one of the two stereo signals (L+R, L-R) is complex-filtered by means of a slope,
- complex-modulating the signals,
- separating the baseband stereo sum signal (L+R) and the stereo difference signal (L-R),
- modulating the L-R and the L+R signal, and
- converting the signals from complex signals to real signals.

16. (original) A method as claimed in claim 15, characterized in that the modulated signal is down-sampled by 2 after the second modulation.

17. (original) A method as claimed in claim 15, characterized in that the signal is down-sampled by 2 after the third modulation.

18. (original) A method as claimed in claim 15, characterized in that the real signals are separated into a left and a right stereo signal.